INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2011; **39**:1145–1160
Published online 14 July 2010 in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.690

Two-switch flyback PWM DC-DC converter in continuous-conduction mode

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SUMMARY

The two-switch flyback DC-DC converter is an extended version of the conventional single-switch flyback converter. An additional switch and two clamping diodes serve as a simple, but an effective way to limit the switch overvoltages, which occur in the conventional single-switch flyback converter due to the ringing of the resonant circuit formed by the transformer leakage inductance and the transistor output capacitance. The clamping diodes in the two-switch flyback topology clamp the maximum voltage across each switch equal to the DC input voltage. This paper presents a detailed steady-state analysis and design procedure of the diode-clamped two-switch flyback converter operated in continuous-conduction mode (CCM). The power loss in each component of the two-switch flyback converter is compared with those of the single-switch flyback converters with and without RCD clamp, and is presented in a tabular form. The two-switch flyback converter was bread-boarded to validate the theoretical analysis. Experimental results from a 10 V/30 W, 100 kHz laboratory prototype verified that the maximum switch voltage is limited to the DC input voltage. Copyright © 2010 John Wiley & Sons, Ltd.

Received 28 October 2009; Revised 9 February 2010; Accepted 1 March 2010

KEY WORDS: clamping diodes; DC-DC converters; flyback converters; RCD-clamp flyback converter; transformer leakage inductance; transistor output capacitance; two-switch flyback converters

1. INTRODUCTION

The flyback pulse-width modulated (PWM) DC-DC power converter is a very important circuit in switching mode power supplies (SMPSs) converter for low-power applications [1–18], such as laptops, battery charge equalizers, and telecommunication equipments. The main drawback of the single-switch flyback converter is the high turn-off voltage stress suffered by the switch. The high voltage transients are caused by the resonant behavior of the transformer leakage inductance and the transistor output capacitance, resulting in ringing superimposed on the steady-state switch voltage level. This requires a transistor with higher on-resistance r_{DS}, causing higher conduction loss. The ringing also increases the switching loss. In addition, the switch voltage stress is not easily predictable because it is difficult to determine the magnitude of the ringing during the design stage. In order to alleviate the drawbacks of the single-switch flyback converter, several topologies of the single-switch flyback converter with active-clamp circuit have been proposed to reduce the switching losses by achieving soft switching [7–13]. However, the switches in converters presented in [7–13] suffer from high voltage stress as the maximum voltage across the switch is the sum of the DC input and the reflected DC output voltages. Furthermore, the gate drive circuit is complex as the main switch and the auxiliary switch are driven complimentarily.

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The circuit arrangement with an addition of a power MOSFET and two clamping diodes to the single-switch flyback converter leads to the two-switch flyback PWM DC-DC converter which effectively reduces the switch overvoltage and eliminates the uncertainty of its value [1, 2, 19]. The main objective of this paper is to present a detailed steady-state analysis of the two-switch flyback DC-DC converter operating in continuous-conduction mode (CCM). The switch output capacitance and the transformer leakage inductance are included in the analysis. In addition, a comparison of the losses of the two-switch and the single-switch flyback converters (with and without RCD clamp) is also performed. The two-switch flyback converter has the following features:

- The maximum switch voltage is clamped to the DC input voltage.
- The clamping diodes provide a path to return the transformer leakage energy to the DC input source.
- The transistor turn-off switching loss is reduced.

Section 2 presents the principle of circuit operation and analysis of the diode-clamped two-switch flyback converter. The two-switch flyback converter design procedure is given in Section 3. In Sections 4 and 5, equations for the power losses in the two-switch flyback converter and experimental results are given, respectively. Conclusions follow in Section 6.

2. CIRCUIT OPERATION AND ANALYSIS

2.1. Circuit description

The basic circuits of the two-switch and the conventional single-switch flyback DC-DC converters are shown in Figures 1(a) and (b), respectively. Figure 1(c) shows the circuit of the single-switch flyback converter with an RCD clamp composed of a resistor R_C, a clamp capacitor C_C, and

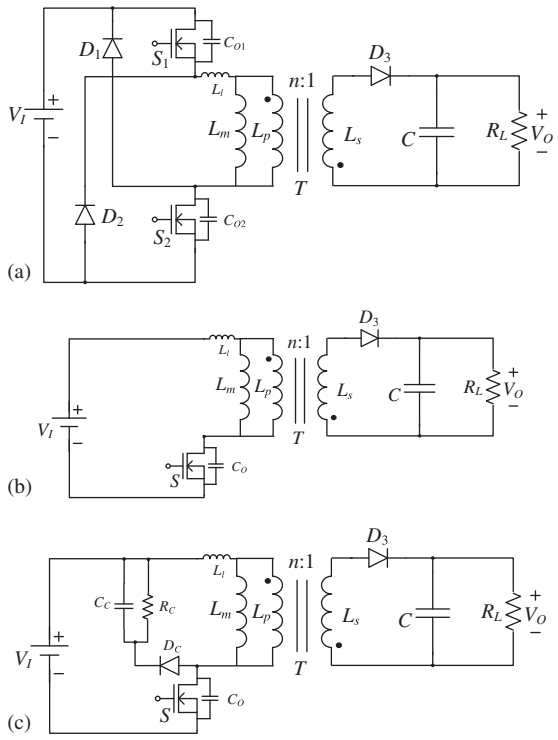

Figure 1. Flyback PWM DC-DC converter circuits: (a) two-switch flyback PWM DC-DC converter; (b) classical single-switch flyback PWM DC-DC converter; and (c) classical single-switch flyback PWM DC-DC converter with RCD clamp.

DOI: 10.1002/cta

a diode D_C. In Figure 1(a), the two switches S_1 and S_2 are n-channel power MOSFETs whose output capacitances are denoted by C_{O1} and C_{O2}, respectively. Clamping diodes D_1 and D_2 are cross connected across the switches and the primary winding. The rectifier diode and the filter capacitor are denoted by D_3 and C, respectively. The input DC voltage and the load resistance are denoted by V_I and R_L, respectively. Both the switches S_1 and S_2 are turned on or off at the same time by a gate driver. The switching period T_s is given by $1/f_s$, where f_s is the switching frequency. The ratio of switch on-time t_{on} to the total period T_s is defined as the switch duty ratio D. The transformer T is modeled as an ideal transformer with its magnetizing inductance L_m (referred to the primary) and the total leakage inductance L_l. To ease the mathematical analysis, the total transformer leakage inductance is referred to the primary. The circuit operation is mainly categorized into six stages.

2.2. *Two-switch flyback converter analysis*

The principle of operation of each stage is explained with the aid of equivalent circuits shown in Figure 2 and the current and voltage waveforms of the converter shown in Figure 3. Before the beginning of switching cycle (time $t = t_0$), the magnetizing inductor current is commutated through the rectifier diode D_3, and all other switches and diodes are off.

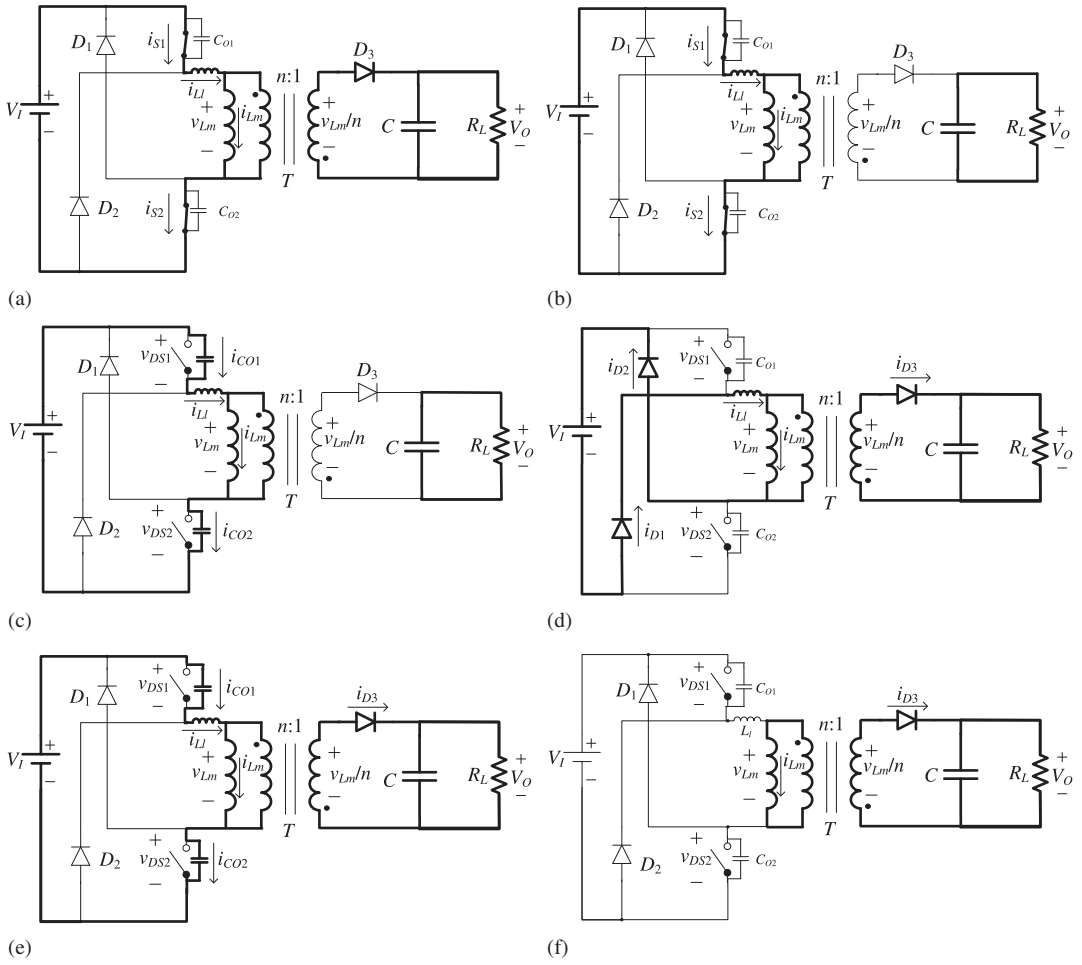

Figure 2. Equivalent circuits of the two-switch flyback converter at different stages of a switching cycle: (a) Stage 1 $[t_0 - t_1]$; (b) Stage 2 $[t_1 - t_2]$; (c) Stage 3 $[t_2 - t_3]$; (d) Stage 4 $[t_3 - t_4]$; (e) Stage 5 $[t_4 - t_5]$; and (f) Stage 6 $[t_5 - t_6]$.

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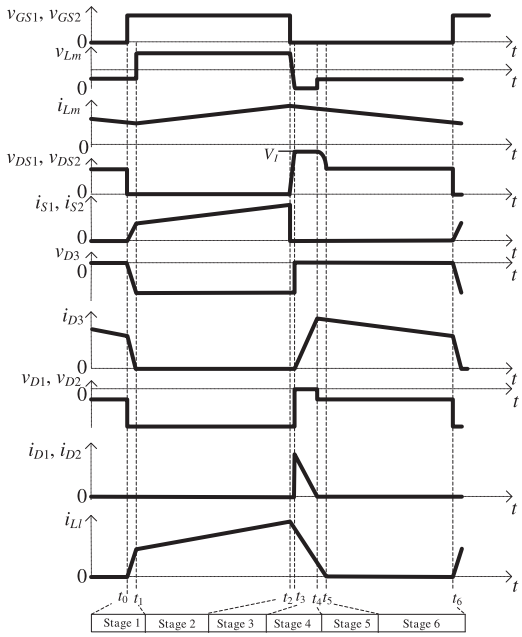

Figure 3. Voltage and current waveforms of the two-switch flyback PWM DC-DC converter in CCM.

Stage 1 [$t_0 < t \leqslant t_1$]: At time $t = t_0$, both the switches S_1 and S_2 are turned on by an external driver. The leakage inductance L_l prevents the instantaneous transfer of magnetizing current from the transformer secondary to primary. Hence, the rectifier diode D_3 remains ON. An equivalent circuit for this stage is shown in Figure 2(a). Since the voltage across the clamping diodes D_1 and D_2 is $-V_I$, the diodes D_1 and D_2 are reverse biased and hence their currents $i_{D1}(t)$ and $i_{D2}(t)$ are zero. The leakage inductance L_l limits the rate of rise of current through the switches S_1 and S_2. The voltage across the magnetizing inductance is $-nV_O$ from which the current through the magnetizing inductance is

$$i_{Lm}(t) = -\frac{nV_O}{L_m}(t - t_0) + i_{Lm}(t_0), \tag{1}$$

where $i_{Lm}(t_0)$ is the initial current of the magnetizing inductance at time $t = t_0$. The voltage across the leakage inductance is $V_I + nV_O$. The current through the leakage inductance and the switches S_1 and S_2 are

$$i_{S1}(t) = i_{S2}(t) = i_{Ll}(t) = \frac{V_I + nV_O}{L_l}(t - t_0) + i_{Ll}(t_0), \quad i_{Ll}(t_0) = 0, \tag{2}$$

where $i_{Ll}(t)$ is the initial value of the current in the leakage inductance at time $t = t$. The current through the switches and the leakage inductance rises linearly with a slope of $(V_I + nV_O)/L_l$. The current through the rectifier diode is

$$i_{D3}(t) = -n[i_{Ll}(t) - i_{Lm}(t)] = -n\left[\frac{V_I L_m + nV_O(L_m + L_l)}{L_m L_l}\right](t - t_0) + ni_{Lm}(t_0). \tag{3}$$

Assuming $L_l \ll L_m$, the rectifier diode current falls linearly with a slope of approximately $-n(V_I + nV_O)/L_l$. The voltages across the switches $v_{S1}(t)$ and $v_{S2}(t)$ are zero. This stage ends at time $t = t_1$, when the current through the leakage inductance equals the magnetizing inductance current and the rectifier diode current reaches zero. Substituting $i_{D3}(t_1) = 0$ into (3), the time period of the first stage is obtained as

$$\Delta t_1 = t_1 - t_0 = \frac{L_l}{V_I + nV_O} i_{Lm}(t_0). \tag{4}$$

DOI: 10.1002/cta

Stage 2 [$t_1 < t \leqslant t_2$]: During this stage the switches S_1 and S_2 are ON and all the diodes D_1, D_2, and D_3 are OFF. An equivalent circuit of this stage is shown in Figure 2(b). The current through the switches, leakage inductance, and the magnetizing inductance is

$$i_{S1}(t)=i_{S2}(t)=i_{Ll}(t)=i_{Lm}(t)=\frac{V_I}{L_m+L_l}(t-t_1)+i_{Lm}(t_1), \tag{5}$$

where $i_{Lm}(t_1)$ is the initial current of the magnetizing inductance at $t=t_1$. The current through the magnetizing inductance, leakage inductance, and the switches rises linearly with a slope of $V_I/(L_m+L_l)$. The voltages across the switches $v_{S1}(t)$ and $v_{S2}(t)$ are zero. The peak current of the magnetizing inductance is

$$i_{Lm}(t_2)=\frac{V_I DT}{L_m+L_l}+i_{Lm}(t_1)=\frac{V_I D}{f_S(L_m+L_l)}+i_{Lm}(t_1). \tag{6}$$

The peak-to-peak value of the ripple current through the magnetizing inductance is

$$\Delta i_{Lm}=i_{Lm}(t_2)-i_{Lm}(t_1)=\frac{V_I D}{f_S(L_m+L_l)}. \tag{7}$$

This stage ends at time $t=t_2$, when both the switches are turned off.

Stage 3 [$t_2 < t \leqslant t_3$]: During this stage, the switches S_1, S_2 and all the diodes D_1, D_2, D_3 are OFF. An equivalent circuit for this stage is shown in Figure 2(c). The magnetizing current (equal to the leakage current) charges the switch output capacitances C_{O1} and C_{O2} in a resonant manner. The current through C_{O1}, C_{O2}, the leakage inductance, and the magnetizing inductance is

$$i_{CO1}(t)=i_{CO2}(t)=i_{Ll}(t)=i_{Lm}(t)=\frac{V_I}{Z_1}\sin\omega_1(t-t_2)+i_{Lm}(t_2)\cos\omega_1(t-t_2), \tag{8}$$

where

$$Z_1=\sqrt{\frac{(L_m+L_l)(C_{O1}+C_{O2})}{C_{O1}C_{O2}}}, \tag{9}$$

and

$$\omega_1=\sqrt{\frac{C_{O1}+C_{O2}}{(L_m+L_l)C_{O1}C_{O2}}}, \tag{10}$$

Assuming $C_{O1}=C_{O2}=C_O$, the switch voltages are

$$v_{DS1}(t)=v_{DS2}(t)=v_{CO1}(t)=v_{CO2}(t)=\frac{i_{Lm}(t_2)Z_1}{2}\sin\omega_1(t-t_2)-\frac{V_I}{2}\cos\omega_1(t-t_2). \tag{11}$$

This stage ends at time $t=t_3$, when the voltage across each switch equals V_I, thus turning on the clamping diodes D_1 and D_2.

Stage 4 [$t_3 < t \leqslant t_4$]: During this stage, the switches S_1 and S_2 are OFF and all the diodes D_1, D_2, and D_3 are ON. An equivalent circuit for this stage is depicted in Figure 2(d). The voltage across each switch is clamped to V_I+V_F, where V_F is the forward voltage of the clamping diode. The current through the leakage inductance charge the input voltage source V_I via clamping diodes D_1 and D_2 given by

$$i_{D1}(t)=i_{D2}(t)=i_{Ll}(t)=-\frac{(V_I-nV_O)}{L_l}(t-t_3)+i_{Ll}(t_3), \tag{12}$$

where $i_{Ll}(t_3)$ is the initial current of the leakage inductance at time t_3. This mode is referred to as regenerative clamping mode. This stage ends at time $t=t_4$, when the rectifier diode current $i_{D3}(t)$ equals the reflected magnetizing inductance current $ni_{Lm}(t)$, thereby turning off the clamping diodes D_1 and D_2.

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Stage 5 [$t_4 < t \leqslant t_5$]: During this stage, the switches S_1, S_2 and the diodes D_1, D_2 are OFF. The diode D_3 is ON. An equivalent circuit for this stage is depicted in Figure 2(e). The resonant current through the leakage inductance L_l and the switch output capacitances C_{O1} and C_{O2} is

$$i_{Ll}(t) = i_{CO1}(t) = i_{CO2}(t) = i_{Ll}(t_4)\cos\omega_2(t-t_4), \tag{13}$$

where $i_{Ll}(t_4)$ is the initial current of the leakage inductance at time instant t_4. The voltage across the leakage inductance is

$$v_{Ll}(t) = -i_{Ll}(t_4)Z_2\sin\omega_2(t-t_4), \tag{14}$$

where

$$Z_2 = \sqrt{\frac{L_l(C_{O1}+C_{O2})}{C_{O1}C_{O2}}}, \tag{15}$$

and

$$\omega_2 = \sqrt{\frac{C_{O1}+C_{O2}}{L_l C_{O1}C_{O2}}}. \tag{16}$$

The voltages across the switches are

$$v_{DS1}(t) = v_{DS2}(t) = v_{CO1}(t) = v_{CO2}(t) = V_I - i_{Ll}(t_4)\sin\omega_2(t-t_4). \tag{17}$$

This stage ends at time $t = t_6$, when the leakage inductance current $i_{Ll}(t)$ drops to zero.

Stage 6 [$t_5 < t \leqslant t_6$]: During this stage, the switches S_1, S_2, the clamping diodes D_1, D_2 are OFF, and the rectifier diode D_3 is ON. An equivalent circuit for this stage is depicted in Figure 2(f). This stage is similar to Stage 5 except that the resonance between C_{O1}, C_{O2}, and L_l has stopped. The voltage across the magnetizing inductance is $-nV_O$. The current through the magnetizing inductance is

$$i_{Lm}(t) = -\frac{nV_O}{L_m}(t-t_5) + i_{Lm}(t_5), \tag{18}$$

where $i_{Lm}(t_5)$ is the initial current of the magnetizing inductance at t_5. The rectifier diode current is

$$i_{D3}(t) = -\frac{n^2V_O}{L_m}(t-t_5) + ni_{Lm}(t_5). \tag{19}$$

Assuming that the switches S_1 and S_2 are identical, the voltages across the switches are

$$v_{DS1}(t) = v_{DS2}(t) = \frac{V_I + nV_O}{2}. \tag{20}$$

Assuming that the clamping diodes D_1 and D_2 are identical, the voltages across the clamping diodes are

$$v_{D1}(t) = v_{D2}(t) = \frac{nV_O - V_I}{2}. \tag{21}$$

The current through the switches $i_{S1}(t)$, $i_{S2}(t)$, the current through the clamping diodes $i_{D1}(t)$, $i_{D2}(t)$, and the leakage inductance current $i_{Ll}(t)$ are zero. This stage ends at time $t = t_6$, when the main switches S_1 and S_2 are turned on, thus completing one complete switching cycle. In Figure 3, the time duration of stages 1, 3, 4, and 5 are exaggerated for better understanding of the converter operation.

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3. TWO-SWITCH FLYBACK DESIGN CONSIDERATIONS

3.1. DC voltage transfer function

Referring to the voltage waveform of the magnetizing inductance in Figure 3 and applying volt–second balance, we have

$$V_I \Delta t_2 = V_I(\Delta t_3 + \Delta t_4) + n V_O(\Delta t_1 + \Delta t_5 + \Delta t_6), \tag{22}$$

from which, the DC voltage transfer function of the converter is

$$M_{VDC} \equiv \frac{V_O}{V_I} = \frac{\Delta t_2 - (\Delta t_3 + \Delta t_4)}{n(\Delta t_1 + \Delta t_5 + \Delta t_6)}. \tag{23}$$

Assuming that the time duration of stages 1, 3, 4, and 5 is very small in comparison with stages 2, and 6, M_{VDC} can be approximated to

$$M_{VDC} \equiv \frac{V_O}{V_I} \approx \frac{\Delta t_2}{n \Delta t_6} = \frac{D}{n(1-D)}. \tag{24}$$

3.2. Device stresses

The selection of components is based on the maximum values of the voltage and current stresses withstood by the switches and the diodes.

Switch stresses: During the fourth stage, the maximum off-state voltage appearing across S_1 and S_2 is given by

$$V_{SM1(\max)} = V_{SM2(\max)} = V_{I(\max)}. \tag{25}$$

During the second stage, the maximum values of the currents through the switches are

$$I_{SM1(\max)} = I_{SM2(\max)} = \frac{I_{O\max}}{n(1-D_{\max})} + \frac{\Delta i_{Lm}}{2}, \tag{26}$$

where $I_{O\max}$ is the maximum DC output current.

Rectifier diode stresses: During the second stage, the maximum value of the diode reverse voltage is

$$V_{DM3(\max)} = \frac{V_I}{n} + V_O. \tag{27}$$

At the end of the fourth stage, the maximum value of the current through the rectifier diode is approximately

$$I_{DM3(\max)} = \frac{I_{O\max}}{1-D_{\max}} + \frac{n\Delta i_{Lm}}{2}. \tag{28}$$

Clamping diode stresses: During the first and the second stage, the maximum values of the clamping diode reverse voltage are

$$V_{DM1(\max)} = V_{DM2(\max)} = V_{I\max}. \tag{29}$$

During the fourth stage, the maximum values of the current through the clamping diodes are

$$I_{DM1(\max)} = I_{DM2(\max)} = \frac{I_{O\max}}{n(1-D_{\max})} + \frac{\Delta i_{Lm}}{2}. \tag{30}$$

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3.3. Two-switch flyback design procedure

(1) *Select transformer turns ratio*: The DC voltage transfer function of the two-switch flyback converter at the boundary between CCM and DCM is given by

$$M_{VDC} = \frac{V_O}{V_I} = \frac{\eta D}{n(1-D)}, \tag{31}$$

from which, the transformer turns ratio is given by

$$n = \frac{\eta D_{\max}}{M_{VDC(\max)}(1-D_{\max})}, \tag{32}$$

where $D_{\max}$ is the maximum duty cycle and $M_{VDC(\max)} = V_O / V_{I(\min)}$. In (32), the maximum value of the duty cycle $D_{\max}$ is taken as 0.5 and M_{VDC} is calculated considering the desired converter efficiency η to be 90%. The peak voltage and current stresses of the devices on either side of the flyback transformer are influenced by n. The current and voltage stresses are minimal when n is such that D is 0.5 [20]. Hence, the value of n is calculated at $D_{\max} = 0.5$. Furthermore, if the converter is operated for $D > 0.5$, the leakage inductance is charged for a longer period of time resulting in a longer duration of the reset period (Stage 4), which in turn delays the transfer of energy stored in the magnetizing inductance to the load, thus reducing the converter efficiency.

(2) *Select flyback transformer magnetizing inductance*: Since the current waveforms of the switches are similar to the switch current of the single-switch flyback converter, the usual method to determine the value of the magnetizing inductance for CCM operation can be used. The minimum value of the magnetizing inductance for CCM operation is given by

$$L_{m(\min)} = \frac{n^2 R_{L\max}(1-D_{\min})^2}{2 f_S} \tag{33}$$

(3) *Select switching devices*: Using (25)–(30), the power MOSFETs and the diodes are selected.

(4) *Select filter capacitor*: Selection of the output filter capacitor is based on the output voltage ripple specification.

$$C = \frac{D_{\max} V_O}{f_S R_{L\min} V_{cpp}}, \tag{34}$$

where V_{cpp} is the peak-to-peak value of the AC component of the voltage across the capacitance, which is approximately

$$V_{cpp} \approx V_r - V_{rcpp}. \tag{35}$$

In (35), V_r is the peak-to-peak value of the output ripple voltage (usually expressed as a percentage of DC output voltage V_O) and $V_{rcpp} = r_C I_{Cpp}$ is the peak-to-peak value of the voltage across the equivalent series resistance (ESR) r_C of the capacitor. The designed capacitor must be able to withstand the rms capacitor current given by

$$I_{Crms} \approx I_O \sqrt{\frac{D}{1-D}}. \tag{36}$$

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The peak-to-peak value of the capacitor current is

$$I_{Cpp} \approx n\Delta i_{Lm} = \frac{nV_O(1-D_{\min})}{f_S(L_m+L_l)}. \tag{37}$$

4. POWER LOSSES AND EFFICIENCY OF THE TWO-SWITCH FLYBACK CONVERTER

Equations for the power losses in the two-switch flyback converter are obtained by assuming that the time duration of stages 1, 3, and 5 are very small. Using (5) and (26), the rms values of the currents through the switches are

$$I_{S1,S2(\text{rms})} = \sqrt{\frac{1}{T_S}\int_{t_0}^{t_2} i_{S1,S2}\,\mathrm{d}t} = \frac{I_O\sqrt{D}}{n(1-D)}. \tag{38}$$

Assuming that the on-resistance of the switches $r_{DS1}=r_{DS2}=r_{DS}$, the total conduction loss in $2r_{DS}$ and primary winding resistance r_{T1} is

$$P_{ST1} = (2r_{DS}+r_{T1})I^2_{S1,S2(\text{rms})} = (2r_{DS}+r_{T1})\frac{DI_O^2}{n^2(1-D)^2}. \tag{39}$$

Assuming that the output capacitance of the switches $C_{O1}=C_{O2}=C_O$ and using Equation (25), the switch capacitive turn-off loss is given by

$$P_{SW} = \tfrac{1}{2}f_S(2C_O)V^2_{SM} = f_S C_O V_I^2. \tag{40}$$

Using Equations (19) and (28), the rms value of the current through the rectifier diode is

$$I_{D3(\text{rms})} = \sqrt{\frac{1}{T_S}\int_{t_2}^{t_6} i_{D3}\,\mathrm{d}t} = \frac{I_O}{\sqrt{1-D}}. \tag{41}$$

The total conduction loss in the forward resistance R_{F3} of the rectifier diode and the secondary winding resistance r_{T2} is

$$P_{DT2} = (R_{F3}+r_{T2})I^2_{D3(\text{rms})} = \frac{(R_{F3}+r_{T2})I_O^2}{1-D} \tag{42}$$

The average rectifier diode current $I_{D3}=I_O$, resulting in the rectifier diode loss associated with the forward voltage of the rectifier diode V_{F3}

$$P_{VF3} = V_{F3}I_{D3} = V_{F3}I_O. \tag{43}$$

Using Equations (12) and (30), the rms values of the currents through the clamping diodes are

$$I_{D1,D2(\text{rms})} = \sqrt{\frac{1}{T_S}\int_{t_3}^{t_4} i_{D1,D2}\,\mathrm{d}t} = \frac{I_O}{n(1-D)}\sqrt{\frac{\Delta t_4}{T_S}}. \tag{44}$$

Assuming that the forward resistances of the clamping diodes $R_{F1}=R_{F2}=R_F$ and $\Delta t_4 = 10\%T_s$, the total conduction loss in $2R_F$ is

$$P_{RF} = (2R_F)I^2_{D1,D2(\text{rms})} = (2R_F)\frac{\Delta t_4}{T_S}\left[\frac{I_O^2}{n^2(1-D)^2}\right] \approx \frac{0.2R_F I_O^2}{n^2(1-D)^2}. \tag{45}$$

The average values of the clamping diode currents $I_{D1}=I_{D2}=I_D=I_I+I_O/n$, resulting in

$$I_{D1}=I_{D2}=I_D=\frac{1}{T_S}\int_{t_3}^{t_4} i_D\,\mathrm{d}t = \frac{I_O}{n(1-D)}\frac{\Delta t_4}{T_S}. \tag{46}$$

DOI: 10.1002/cta

Table I. List of components and their specifications.

Parameter	Two-switch flyback converter		Single-switch flyback converter [19]	
	Calculated value	Component	Calculated value	Component
Power MOSFET switches		IRF510		IRF840
Maximum voltage stress	$V_{SM1(\max)} = V_{SM2(\max)} = V_{I\max} = 60\,\text{V}$	100 V	$V_{SM(\max)} = V_I + nV_O + I_{SM}Z_O = 348\,\text{V}$	500 V
Maximum current stress	$I_{SM1(\max)} = I_{SM2(\max)} = [I_O/n(1-D_{\max})] + (\Delta i_{Lm(\max)}/2) = 1.99\,\text{A}$	5 A	$I_{SM(\max)} = [I_O/n(1-D_{\max})] + (\Delta i_{Lm(\max)}/2) = 1.99\,\text{A}$	8 A
Maximum drain-to-source on-resistance	$r_{DS(\max)}$	0.54 Ω	$r_{DS(\max)}$	0.85 Ω
MOSFET drain-to-source capacitance	C_{DS}	60 pF	C_{DS}	120 pF
Rectifier diode		MBR10100		MBR10100
Maximum voltage stress	$V_{DM3(\max)} = V_{I\max}/n + V_O = 30\,\text{V}$	100 V	$V_{DM3(\max)} = V_{I\max}/n + V_O = 30\,\text{V}$	100 V
Maximum current stress	$I_{DM3(\max)} = n\Delta i_{Lm(\max)} = 5.97\,\text{A}$	10 A	$I_{DM3(\max)} = n\Delta i_{Lm(\max)} = 5.97\,\text{A}$	10 A
Diode forward voltage	V_{F3}	0.65 V	V_{F3}	0.65 V
Diode forward resistance	R_{F3}	20 mΩ	R_{F3}	20 mΩ
Clamping diodes		MBR10100	—	—
Maximum voltage stress	$V_{DM1(\max)} = V_{DM2(\max)} = V_{I\max} = 60\,\text{V}$	100 V	—	—
Maximum current stress	$I_{DM1(\max)} = I_{DM2(\max)} = [I_O/n(1-D_{\max})] + (\Delta i_{Lm(\max)}/2) = 1.99\,\text{A}$	10 A	—	—
Diode forward voltage	$V_{F1} = V_{F2}$	0.65 V	—	—
Diode forward resistance	$R_{F1} = R_{F2}$	20 mΩ	—	—
Flyback transformer		Magnetics Pot Core		Magnetics Pot Core
Core number		0P-43622		0P-43622
Primary winding magnetizing inductance	$L_{mp} = 650\,\mu\text{H}$	641 μH	$L_{mp} = 650\,\mu\text{H}$	641 μH
Secondary winding magnetizing inductance	$L_{ms} = 75.2\,\mu\text{H}$	71.2 μH	$L_{ms} = 75.2\,\mu\text{H}$	71.2 μH
Number of primary winding turns	$n_p = 36$	36	$n_p = 36$	36
Number of secondary winding turns	$n_s = 12.24$	12	$n_s = 12.24$	12
Primary-to-secondary turns ratio	$n = 2.94$	3	$n = 2.94$	3
Primary leakage inductance	L_{lp}	14.4 μH	L_{lp}	14.4 μH
Secondary leakage inductance	L_{ls}	2.98 μH	L_{ls}	2.98 μH
Total leakage inductance (primary)	L_l	14.73 μH	L_l	14.73 μH
Primary winding resistance	r_{T1}	98 mΩ	r_{T1}	98 mΩ
Secondary winding resistance	r_{T2}	29.9 mΩ	r_{T2}	29.9 mΩ
Magnetizing inductance ESR	r_L	170 mΩ	r_L	170 mΩ
Length of air gap	$l_g = 0.5\,\text{mm}$	0.5 mm	$l_g = 0.5\,\text{mm}$	0.5 mm

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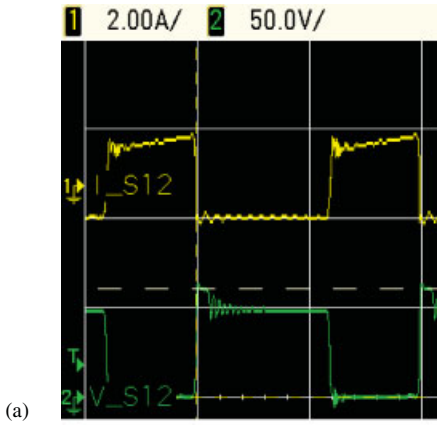
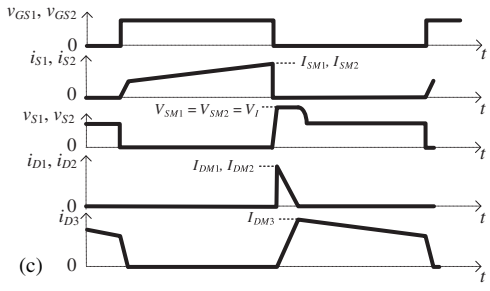


(a)

(b)



(c)

Figure 4. Experimental results of the two-switch switch flyback converter at $V_I = 60\,\text{V}$ and $P_O = 30\,\text{W}$: (a) top trace: switch current waveforms i_{S1}, i_{S2} (2 A/div.); bottom trace: switch drain-to-source voltage waveforms v_{DS1}, v_{DS2} (50 V/div.). Horizontal scale: 5 μs/div; (b) top trace: clamping diode current waveforms i_{D1}, i_{D2} (2 A/div.); bottom trace: rectifier diode current waveform i_{D3} (10 A/div.). Horizontal scale: 5 μs/div.; and (c) key theoretical waveforms of the two-switch flyback converter.

Assuming that the forward voltages of the clamping diodes $V_{F1} = V_{F2} = V_F$ and $\Delta t_4 = 10\% T_s$, the loss associated with the forward voltages of two clamping diodes is

$$P_{VF} = 2V_F I_D = \frac{2V_F I_O}{n(1-D)} \frac{\Delta t_4}{T} \approx \frac{0.2V_F I_O}{n(1-D)}. \tag{47}$$

Using Equations (5), (18), and (26), the rms value of the current through the magnetizing inductance is approximately

$$I_{Lm(\text{rms})} \approx I_I + \frac{I_O}{n} = \frac{I_O}{n(1-D)}. \tag{48}$$

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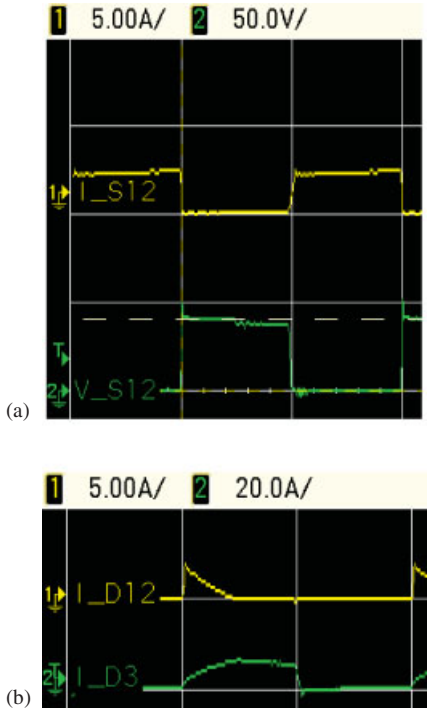

Figure 5. Experimental results of the two-switch switch flyback converter at $V_I = 40\,\text{V}$ and $P_O = 30\,\text{W}$: (a) top trace: switch current waveforms i_{S1}, i_{S2} (5 A/div.); bottom trace: switch drain-to-source voltage waveforms v_{DS1}, v_{DS2} (50 V/div.). Horizontal scale: 5 µs/div. and (b) top trace: clamping diode current waveforms i_{D1}, i_{D2} (5 A/div.); bottom trace: rectifier diode current waveform i_{D3} (20 A/div.). Horizontal scale: 5 µs/div.

The power loss in the ESR r_L of the magnetizing inductance is

$$P_{rL} = r_L I_{Lm(\text{rms})}^2 = \frac{r_L I_O^2}{n^2(1-D)^2}. \tag{49}$$

The total power loss in the two-switch flyback converter is

$$P_{LS} = P_{ST1} + P_{SW} + P_{DT2} + P_{VF3} + P_{RF} + P_{VF} + P_{rL}. \tag{50}$$

The efficiency of the two-switch flyback converter is

$$\eta \equiv \frac{P_O}{P_I} = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + \dfrac{P_{LS}}{P_O}}. \tag{51}$$

The equations for the power losses of the single-switch flyback converter for CCM can be found in [19].

The ratio of the conduction loss in the transistor of the single-switch flyback converter $P_{rDS(1\text{Switch})}$ to the conduction loss in both the transistors $P_{rDS(2\text{Switch})}$ of the two-switch flyback converter is

$$\frac{P_{rDS(1\text{Switch})}}{P_{rDS(2\text{Switch})}} = \frac{r_{DS(1\text{Switch})}}{2r_{DS(2\text{Switch})}} = \frac{1}{2}\left(\frac{V_{BD(1\text{Switch})}}{V_{BD(2\text{Switch})}}\right)^{2.2} = \frac{1}{2}\left(\frac{V_{I\max} + nV_O + V_{pk(\text{ring})}}{V_{I\max}}\right)^{2.2} \tag{52}$$

where $r_{DS(1\text{Switch})}$ is the MOSFET on-resistance in the single-switch flyback converter, $r_{DS(2\text{Switch})}$ is the MOSFET on-resistance in the two-switch flyback converter, $V_{BD(1\text{Switch})}$ is the MOSFET breakdown voltage in the single-switch flyback converter, $V_{BD(2\text{Switch})}$ is the MOSFET breakdown voltage in the two-switch flyback converter, and $V_{pk(\text{ring})}$ is the magnitude of the ringing. Thus

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the conduction loss in both the transistors $P_{rDS(2Switch)}$ of the two-switch flyback converter is likely to be lower than the conduction loss in the transistor of the single-switch flyback converter $P_{rDS(1Switch)}$.

5. EXPERIMENTAL RESULTS

The two-switch flyback converter is designed for the following specifications:

- Input voltage: 50 ± 10 VDC
- Output voltage: 10 VDC
- Maximum output power: 30 W (3 W min)
- Switching frequency: 100 kHz

The results obtained from the design procedure presented in Section 3 are given in Table I. The theoretical voltage and current waveforms of the two-switch flyback converter shown in Figure 3 are experimentally verified. The experimental voltage and current waveforms of the two-switch flyback converter at full load and maximum and minimum input voltages of 60 and 40 V are presented in Figures 4 and 5, respectively. The maximum voltage across the power MOSFET switches is clamped to 60 V for $V_I = 60$ V and 40 V for $V_I = 40$ V as shown in Figures 4(a) and 5(a), respectively. The switch currents are shown in Figures 4(a) and 5(a), and the clamping diode currents along with the output rectifier diode current are shown in Figures 4(b) and 5(b) for V_I equal to 60 V and 40 V, respectively. The clamping diodes D_1 and D_2 turn off at zero current.

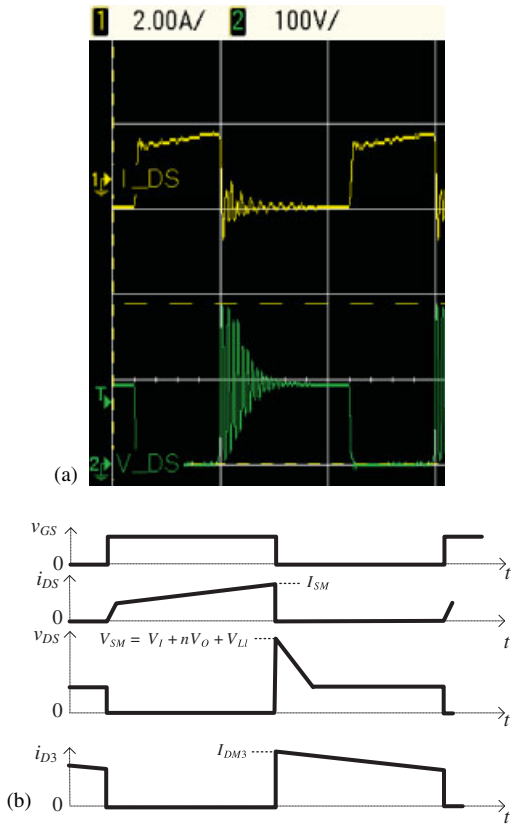

Figure 6. (a) Experimental results of the single-switch switch flyback converter at $V_I = 60$ V and $P_O = 30$ W: top trace: switch current waveform i_{DS} (2 A/div.); bottom trace: switch drain-to-source voltage waveform v_{DS} (100 V/div.). Horizontal scale: 5 μs/div. and (b) key theoretical waveforms of the classical single-switch flyback converter.

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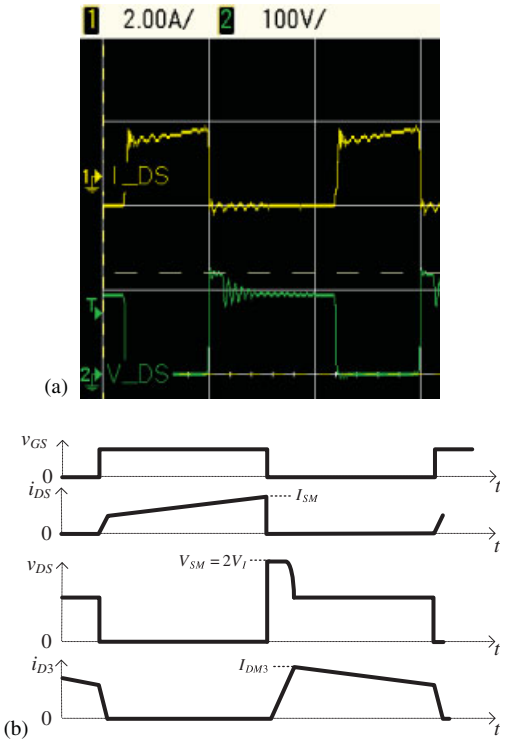

Figure 7. (a) Experimental results of the single-switch flyback converter with an RCD clamp at $V_I = 60\,\text{V}$ and $P_O = 30\,\text{W}$: top trace: switch current waveform i_{DS} (2 A/div.); bottom trace: switch drain-to-source voltage waveform v_{DS} (100 V/div.). Horizontal scale: 5 μs/div. and (b) key theoretical waveforms of the classical single-switch flyback converter with RCD clamp circuit.

Figures 6 and 7 show the experimental and theoretical current and voltage waveforms of the switch in the single-switch flyback converter without and with an RCD clamp circuit, respectively. From the experimental voltage waveform of the switch shown in Figure 6(a), it can be seen that the voltage stress of the switch is unpredictable due to the resonance caused by the transformer leakage inductance and the switch output capacitance. The voltage across the switch in the single-switch flyback converter with an RCD passive clamp is clamped to $2V_I = 120\,\text{V}$ as shown in Figure 7(a) and is in excellent agreement with the theoretical waveform shown in Figure 7(b). However, the additional loss in the clamping circuit reduces the efficiency of the single-switch flyback converter with RCD clamp. The parameters listed in Table I are measured using Hewlett Packard 4275A Multi-Frequency LCR meter. Table II gives the comparison of losses of the two-switch and the single-switch flyback converters for full load and light load conditions, respectively. From Table II, it is clearly seen that the maximum voltage stress of the power MOSFET in the single-switch flyback converter is predicted to be 348 V. A MOSFET with higher voltage rating (IRF840, 500 V, 0.85Ω) is used in the single-switch flyback converter, whereas a MOSFET with lower voltage rating (IRF510, 100 V, 0.54Ω) is safely used in the two-switch topology.

Figure 8 compares the efficiencies of the two-switch flyback converter and the single-switch flyback converter (with and without RCD clamp) versus the output power. A plot of theoretical efficiency predicted using the equations given in Section 4 is shown in Figure 8 and is fairly in good agreement with the measured efficiency of the two-switch flyback converter circuit. The total on-resistance of two power MOSFETs used in the two-switch topology is slightly larger than that of the on-resistance of the single MOSFET used in the single-switch version due to which the conduction losses in the two-switch flyback converter are only about 1.25 times than that of the single-switch flyback converter. From Table II, it can be clearly seen that the overall losses in the two-switch flyback converters are lesser than that of the single-switch flyback converter largely due to the reduced switching losses in the two-switch flyback converter.

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Table II. Comparison of power losses of the two-switch and the single-switch flyback converters.

		$P_O = 30$W		$P_O = 10$W	
	Symbol	Loss (W)	% of P_O	Loss (W)	% of P_O
Two-switch flyback converter					
MOSFET conduction loss	$2P_{rDS}$	1.6066	5.35	0.1758	1.758
MOSFET switching loss	$2P_{sw}$	0.0216	0.072	0.0216	0.216
Rectifier diode loss	P_{D3}	2.27	7.56	0.6864	6.864
Clamping diode loss	$2P_{D1D2}$	0.8975	2.99	0.1522	1.522
Primary winding resistance loss	P_{rT1}	0.1458	0.486	0.0162	0.162
Secondary winding resistance loss	P_{rT2}	0.4894	1.63	0.0538	0.538
Magnetizing inductance ESR loss	P_{rL}	0.562	1.87	0.0624	0.624
Total power losses	P_{LS}	5.99	19.958	1.168	11.168
Efficiency		83.35%		89.95%	
Single-switch flyback converter [19]					
MOSFET conduction loss	P_{rDS}	1.264	4.21	0.1405	1.405
MOSFET switching loss	P_{sw}	3.63	12.1	0.751	7.51
Rectifier diode loss	P_{D3}	2.27	7.56	0.6864	6.86
Clamping diode loss	—	—	—	—	—
Primary winding resistance loss	P_{rT1}	0.1458	0.486	0.0313	0.313
Secondary winding resistance loss	P_{rT2}	0.4894	1.63	0.0538	0.538
Magnetizing inductance ESR loss	P_{rL}	0.562	1.87	0.0624	0.624
Total power losses	P_{LS}	8.36	27.856	1.725	17.25
Efficiency		78.2%		85.28%	
Single-switch flyback converter with RCD clamp					
MOSFET conduction loss	P_{rDS}	1.264	4.21	0.1405	1.405
MOSFET switching loss	P_{sw}	0.1107	0.369	0.0625	0.625
Rectifier diode loss	P_{D3}	2.27	7.56	0.6864	6.86
Clamping diode loss	—	—	—	—	—
Primary winding resistance loss	P_{rT1}	0.1458	0.486	0.0313	0.313
Secondary winding resistance loss	P_{rT2}	0.4894	1.63	0.0538	0.538
Magnetizing inductance ESR loss	P_{rL}	0.562	1.87	0.0624	0.624
RCD Snubber Circuit	P_{RCD}	4.707	15.69	1.451	14.51
Total power losses	P_{LS}	9.54	31.815	2.487	24.87
Efficiency		75.87%		80.08%	

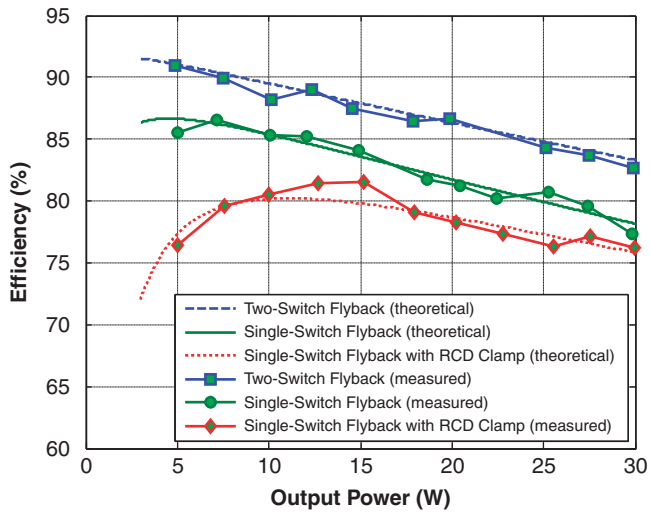

Figure 8. Efficiencies of the two-switch flyback and the single-switch flyback converters.

DOI: 10.1002/cta

6. CONCLUSIONS

This paper has presented the steady-state analysis of the two-switch flyback converter for CCM, taking switch output capacitance and transformer leakage inductance into account. Incorporation of an additional switch and two clamping diodes into the classical single-switch flyback topology provides a simple mechanism to limit the switch overvoltage. This turn-off voltage stress is predictable and well determined. The theoretical analyses have been verified by experimental results. Clamping of the switch overvoltage is achieved. The power transistors are turned on under reduced stresses. These stresses are also well determined. The uncertainty of the voltage stress in the single-switch flyback converter is removed in the two-switch flyback converter at the expense of an additional switch and two clamping diodes. The analysis and experimental results provide a basic understanding of the converter behavior. The two-switch flyback converter is a simple topology with a high practical value for low-power applications. The main disadvantage of the two-switch flyback converter is that it needs a gate-drive circuit that is capable of driving a high-side power MOSFET. The analysis of the two-switch flyback converter with nonlinear parasitic components and comparing the performance of the two-switch flyback converter with the soft-switching flyback converters is recommended for future work.

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DOI: 10.1002/cta